DATASHEET

CADENCE CHIP PLANNING SYSTEM

The Cadence® Chip Planning System is an enterprise-level solution that enables multiple dispersed project teams to perform early chip planning using models of internally developed intellectual property. An IP model generator populating a central server allows internal and external chip design teams to perform "what-if" estimations of die size, power consumption, performance, and total chip cost. The Cadence Chip Planning System provides a complete solution to rapidly explore, plan, and estimate chip design projects utilizing accurate models of a company's own IP, processes, and libraries.

CADENCE CHIP PLANNING SYSTEM

In order to deliver increasingly complex chips on the same schedules, chip design projects must be able to take advantage of re-used IP—both internally and externally developed. Companies implementing chips from multiple design teams have developed large suites of IP that often span different objectives—such as performance, power, size, and functionality—in addition to different processes. The challenge becomes one of helping design teams choose the proper IP when planning their chip projects.

A client-server model enables chip design teams to explore a variety of IP, architectures, memories, and processes, in order to determine how they will meet their project's goals. An IP modeler also enables enterprises to populate the system with accurate high-level models and datasheets suitable for pre-RTL exploration. This data, which can be optionally supplemented with the industry-leading IP ecosystem at ChipEstimate.com, is hosted on the enterprise's server. The server can then be accesses by dispersed chip design teams (both internal and external).

This approach enables simple-to-use early exploration of performance, power, and size utilizing enterprise-specific IP. Typical users include: technical team members (design architects, chip integrators, design leads, and engineering management), as well as business team members (field sales consultants, technical marketing, IC component procurement, RFQ responders, and executive management). It is useful for large fabless semiconductor companies, integrated device manufacturers (IDMs), ASIC vendors, and design service providers.

BENEFITS

- For integrated device manufacturers (IDMs) and large fabless semiconductor companies
  - Facilitate use of your internally developed process libraries and digital, analog, and mixed-signal IP in diverse chip design projects
  - Control over data access—what IP and libraries, and what type of information (technical, economic)—is available to each user
- For ASIC vendors and design service providers
  - Field sales consultants can always access the latest data in order to deliver accurate project estimates and quotes quickly
  - Enable customers to access the technical data for your IP and library models for chip planning
- Improve predictability of success by closing early on a specification that best balances size, power, and costs, using real IP, process, and architecture data
- Estimate power at the architectural level and plan the block- and chip-level power strategies, model different power modes, and generate a CPF file to drive downstream implementation

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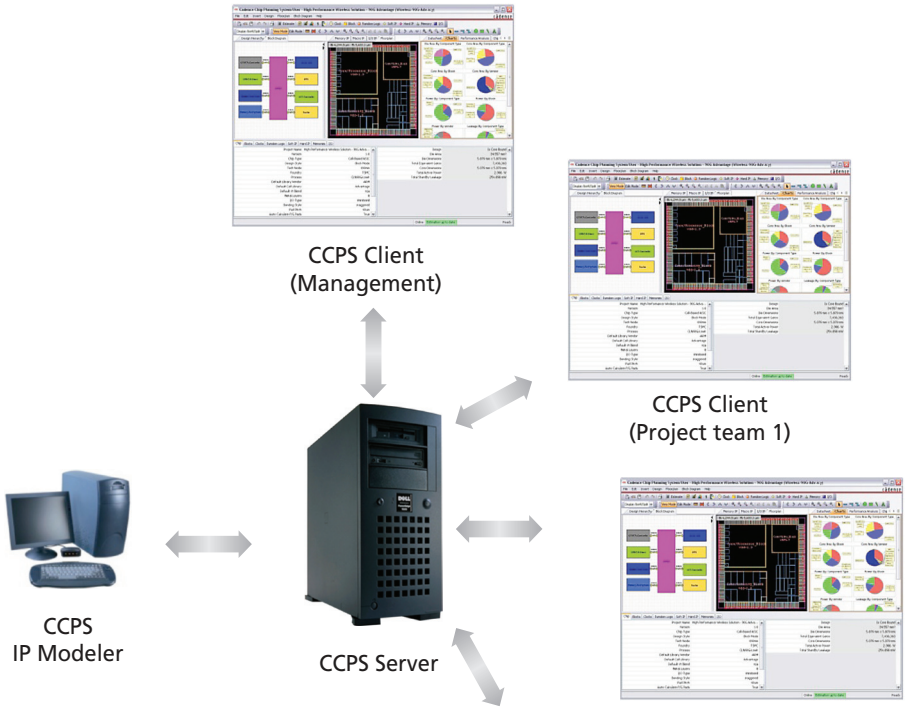

Cadence Chip Planning System

Complete infrastructure for chip planning and estimation using proprietary IP

- Centralized tracking of chip estimations and IP usage to better understand consumption patterns and customer needs
- Reduced implementation risk delivered by early planning followed by a convergent flow—the architecture and library data is passed forward to drive implementation tools, which feed back implemented block data to refine accuracy of the model and drive in-project decisions
- The Cadence Chip Planning System client is easy to use for technical and non-technical users alike, enabling collaboration and communication between the business and technical teams starting with early planning and continuing throughout the course of the project

FEATURES

The Cadence Chip Planning System operates in a client-server model. The client is the CCPS User Estimation application on the project team's Windows or Linux desktop. On the server side, the CCPS IP Modeler generates accurate models and datasheets for chip planning and estimation, populating the CCPS Server with all the data needed for the client application to estimate chip design projects.

CADENCE CHIP PLANNING SYSTEM SERVER

A centralized server application for hosting the enterprise's IP and library models, the Cadence Chip Planning System Server enables dispersed users, both internal and external to the enterprise, to always have access to up-to-date estimation data.

- Centralized server to host IP, library, and memory models
- Web-based IP catalog management system
- Up-to-date model information available to internal and/or external users
- Access to specific models, technical specs, and economic data is controllable per user
- Generate reports on overall IC designs
- Track IP usage by chip and by user
- Custom and tunable process models for highest degree of technical accuracy
- Tunable economic models for more accurate business lifecycle planning
- Can optionally include the full ChipEstimate.com ecosystem of IP

CADENCE CHIP PLANNING SYSTEM USER

The Cadence Chip Planning System User client application enables diverse users such as design teams, technical marketing, field sales consultants, and management to access up-to-date model information from the CCPS Server in order to quickly and accurately estimate and plan chip design projects.

- Estimate design size
- Estimate design power (dynamic and leakage)
- Compare size, power, and performance of multiple designs or design variations
- Estimate performance achievability in specific manufacturing processes with specific IP components
- Create and edit a block diagram of the design, use drag & drop for blocks, and drawing tools for connectivity
- Edit the floorplan view to analyze impact of movement and rotation on size, power, performance, and cost

- Create power profiles with various modes, assign percent-active time for modes
- Easily enable advanced power management techniques, including power shutoff, multi-supply/multi-voltage, and clock gating, while measuring the size and power impact of these techniques
- If enabled by the server:
  - Economic analysis, including yield-affected wafer costs yield, package costs, test & assembly costs, Non-Recurring Engineering (NRE) charges, plotted along economic lifecycle tables and graphs
  - Generate complete IC economic analysis reports and budgetary quotes
- Bi-directional interface to Cadence Encounter RTL Compiler synthesis solution, feeding forward SDC, module definitions, floorplan guidance, and synthesis scripts; feed back synthesized gate counts of random logic blocks and compare versus earlier estimates
- Bi-directional interface to Cadence Encounter® Digital Implementation System, feeding forward SDC, module definitions, floorplan guidance, and implementation scripts; feed back implementation metrics to enable economic analysis and compare versus earlier estimates

CADENCE CHIP PLANNING SYSTEM IP MODELER

In order to populate the server with data that can be used for estimation, the enterprise's IP, libraries and memories must be properly modeled. The Cadence Chip Planning System IP Modeler utilizes standard design kits and memory compilers to generate accurate macro models for use in estimation.

- The same proven-accurate modeling technology used for the extensive ChipEstimate.com suite of models, on-site at the enterprise with full ability to tune and customize
- Characterizes cell libraries and processes using industry-standard Liberty and LEF data
- Memory compilers are analyzed and exercised to produce accurate polynomial models
- Modeler scaling technology enables quick-and-easy modeling of process migration

STANDALONE CLIENT-ONLY VERSION

For fabless companies and design houses using commercially available IP and process technology, the Cadence InCyte Chip Estimator delivers fast, accurate, and easy to use estimation to drive "what-if" exploration and planning. For more information on this version, please consult the Cadence InCyte Chip Estimator datasheet.

SYSTEM SPECIFICATION

- Windows XP, Windows XP Pro, and Windows Vista
- Linux (32-bit, 64-bit) RHEL 4.0, 5.0, SLES 10, 9
- Sun Solaris (32-bit, 64-bit) Solaris 10

Visit www.ChipEstimate.com to register and search through 7000 pieces of IP from over 200 IP Providers and Foundries.

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